

## Features

- Compatible with MCS<sup>®</sup>51 Products
- 2K/4K Bytes of In-System Programmable (ISP) Flash Program Memory
  - Serial Interface for Program Downloading
  - Endurance: 10,000 Write/Erase Cycles
- 2.7V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial UART Channel
- Direct LED Drive Outputs
- On-chip Analog Comparator with Selectable Interrupt
- 8-bit PWM (Pulse-width Modulation)
- Low Power Idle and Power-down Modes
- Brownout Reset
- Enhanced UART Serial Port with Framing Error Detection and Automatic Address Recognition
- Internal Power-on Reset
- Interrupt Recovery from Power-down Mode
- Programmable and Fuseable x2 Clock Option
- Four-level Enhanced Interrupt Controller
- Power-off Flag
- Flexible Programming (Byte and Page Modes)
  - Page Mode: 32 Bytes/Page
- User Serviceable Signature Page (32 Bytes)

## 1. Description

The AT89S2051/S4051 is a low-voltage, high-performance CMOS 8-bit microcontroller with 2K/4K bytes of In-System Programmable (ISP) Flash program memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89S2051/S4051 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications. Moreover, the AT89S2051/S4051 is designed to be function compatible with the AT89C2051/C4051 devices, respectively.

The AT89S2051/S4051 provides the following standard features: 2K/4K bytes of Flash, 256 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a six-vector, four-level interrupt architecture, a full duplex enhanced serial port, a precision analog comparator, on-chip and clock circuitry. Hardware support for PWM with 8-bit resolution and 8-bit prescaler is available by reconfiguring the two on-chip timer/counters. In addition, the AT89S2051/S4051 is designed with static logic for operation down to zero frequency and supports two software-selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the disabling all other chip functions until the next external interrupt or hardware reset.



**8-bit  
Microcontroller  
with 2K/4K  
Bytes Flash**

**AT89S2051  
AT89S4051**

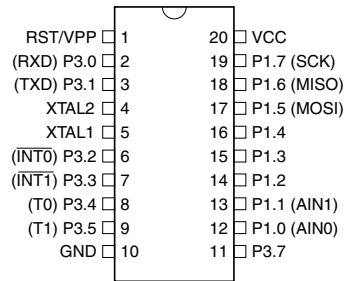
**Preliminary**



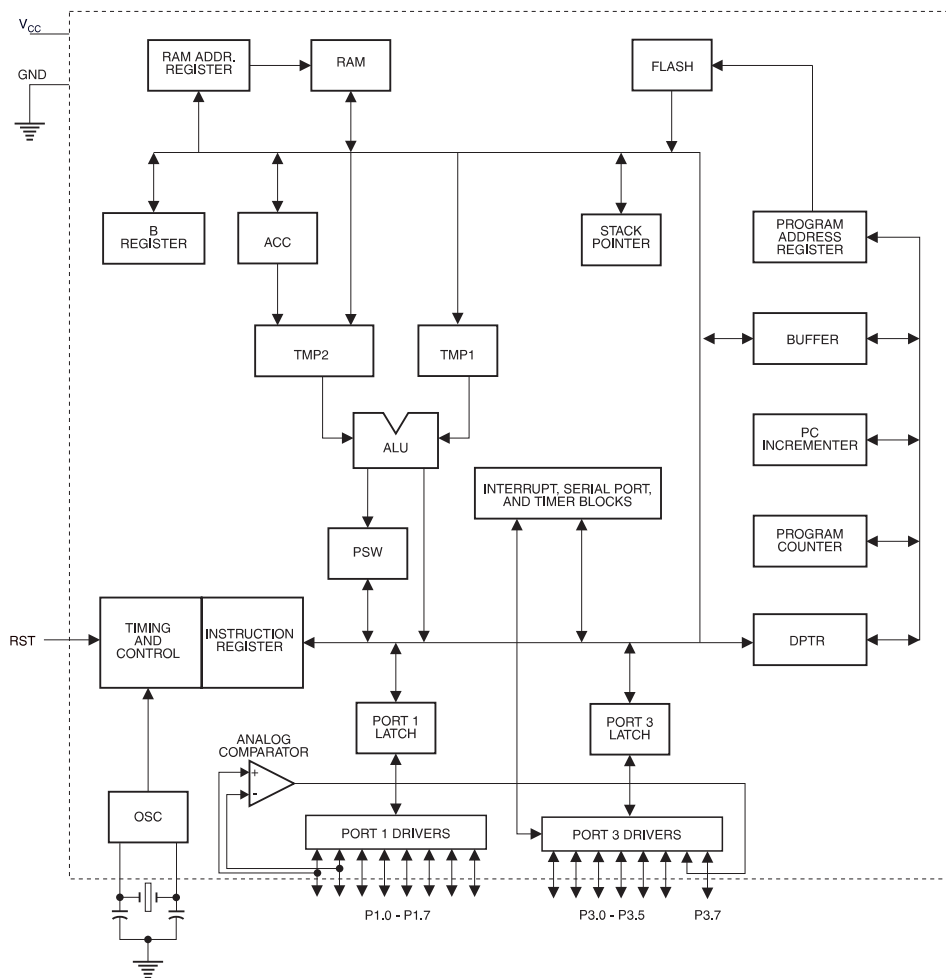
The on-board Flash program memory is accessible through the ISP serial interface. Holding RST active forces the device into a serial programming interface and allows the program memory to be written to or read from, unless one or more lock bits have been activated.

## 2. Pin Configuration

### 2.1 20-lead PDIP/SOIC



## 3. Block Diagram



## 4. Pin Description

### 4.1 VCC

Supply voltage.

### 4.2 GND

Ground.

### 4.3 Port 1

Port 1 is an 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current ( $I_{IL}$ ) because of the internal pull-ups.

Port 1 also receives code data during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (Master data output, slave data input pin for ISP channel)
P1.6	MISO (Master data input, slave data output pin for ISP channel)
P1.7	SCK (Master clock output, slave clock input pin for ISP channel)

### 4.4 Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general-purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89S2051/S4051 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)/ PWM output

Port 3 also receives some control signals for Flash programming and verification.

#### 4.5 RST

Reset input. Holding the RST pin high for two machine cycles while the is running resets the device.

Each machine cycle takes 6 or clock cycles.

#### 4.6 XTAL1

Input to the inverting amplifier and input to the internal clock operating circuit.

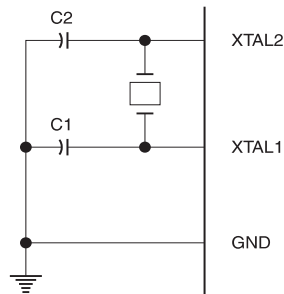
#### 4.7 XTAL2

Output from the inverting amplifier.

### 5. Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip , as shown in [Figure 5-1](#). Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in [Figure 5-2](#). There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Figure 5-1.** Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals  
 = 40 pF ± 10 pF for Ceramic Resonators

**Figure 5-2.** External Clock Drive Configuration

